CLAIMS

1. In a processing system having a processor coupled to a system bus, a method of operating a device, comprising:

instructing the processor to operate with the device;

putting information on the system bus;

retrieving the information with a memory map controller interface;

accessing a template of the device with the memory map controller interface responsive to the information;

putting device information onto an external interface bus according to the information and the template; and

operating the device according to the device information.

2. The method of claim 1, wherein the device is an LCD controller, co-processor, peripheral device, graphic accelerator, imaging device or simply any peripheral with addressable registers or memory.

3. The method of claim 1, wherein the system bus contains an address bus.

4. The method of claim 1, wherein the information comprises a method of operation of the device.

5. The method of claim 4, wherein the method of operation is selected from a group consisting of read and write.

6. The method of claim 1, wherein the information comprises a mode of operation, chip select, access type, and an address.

7. The method of claim 1, wherein the template is selected from a plurality of templates stored in a memory coupled to the system bus, further wherein at least one template is optional on a per access/device type basis.

8. A wireless system, comprising:
an antenna;
an RF processor coupled to the antenna;
a baseband modem processor coupled to the RF processor and to a modem bus;
a processor coupled to a system bus and to the baseband modem processor;
a memory for storing a plurality of templates for devices;
a multiplexer coupled to the memory, the modem bus, and the system bus;
a memory map controller interface for receiving information about devices, retrieving templates from the memory, and providing device information onto an external interface bus according to the received information and the retrieved templates; and
a display controller, coupled to the external interface bus, for responding to the device information.

9. The wireless system of claim 8, further comprising an external device coupled to the external interface bus.

10. The wireless system of claim 8, wherein the information comprises a mode of operation, chip select, access type, and an address.

11. The wireless system of claim 8, wherein the system bus comprises an address bus that carries the information.

12. A processing system for controlling devices via an external interface bus comprising:
a processor coupled to a system bus;
a memory coupled to the system bus for storing templates for describing operating characteristics of the devices; and
a memory map controller interface coupled to the system bus and to an external interface bus.

13. The processing system of claim 12, wherein the memory map controller interface is further characterized as receiving information from the processor via the system bus and receiving templates from the memory via the system bus.

14. The processing system of claim 13, wherein the received information comprises: a mode of operation, chip select, access type, and an address.

15. The processing system of claim 14, wherein the templates comprise data about operating characteristics of the devices.

16. The processing system of claim 13, wherein the templates comprise access protocols of the devices.

17. The processing system of claim 13, wherein at least one of the templates is for a display controller.

18. The processing system of claim 13, wherein the system bus comprises an address bus.

19. A processing system, comprising:
a processor coupled to a system bus;
a memory coupled to the system bus for storing a plurality of templates; and
controller means, coupled to the system bus and to an external interface bus, for responding to information provided by the processor concerning a device by retrieving a template of the plurality of templates and providing the information, in a manner consistent with the retrieved template, on the external interface bus.

20. The processing system of claim 19, wherein each template corresponds to a type of device and a mode of operation for the type of device.

21. The processing system of claim 20, wherein the memory the stores an operating system that identifies devices that are to be accessed.

22. The processing system of claim 21, wherein the information provided by the processor to the controller means specifies a mode of operation.

23. The processing system of claim 22, wherein at least one of the plurality of templates is for a display controller.

24. The processing system of claim 19, wherein the information provided by the processor comprises:

a mode of operation, chip select, access type, and an address.

25. The processing system of claim 19, wherein the templates comprise access protocols of the devices.